Microelectronics Training Environment Proposal: An Analog Design-Based Evolution Perspective

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***Abstract*—This paper summarizes an EDA (Electronic Design Automation) tools-based microelectronics training experience accomplished in the context of IC-Brazil Program. Representing a professional certification proposal in the fields of physics and engineering, the program involves two training phases and a final microelectronics project to be developed through an IC design environment generated for educational purposes from the real conditions of the industry. Supported through financial resources from federal government, IC-Brazil Program experience has promoted the manpower generation with proper knowledge and design skills to attend the electronics design-based semiconductor market.**

I. Introduction

Along the last decades, the rising trend of the semiconductors market in global scale has attracted investments with strategic features for the global economy. This context of investments has generated significant effects on the trade balance, impacting directly on industry production and technological domain, and implying on: (1) innovation engine, (2) skilled jobs, (3) strategic technology (4) rising demand, and (5) added value [1].

Applied in all sectors of the human activity for execution and control of operations, electronics represents an innovation engine (1) and an essential management resource in critical areas (security, logistics, health, transports, communications and energy). Toward this end, it can leverage the generation of new skilled jobs (2) involving wide technical knowledge and specialized practical background. The resulting manpower training can stimulate the search of autonomy in strategic technology (3) for critical sectors (national security, telecommunications and energy). Additionally, the rising demand (4) for devices operating in connection with internet stimulates the development of new applications and functionalities (microprocessors, sensors, transceivers, converters and trackers). Finally, the application of integrated circuits has contributed in a rising percentage in the added value (5) of new technologies.

Considering this global scenery of technology advancement, the exponential development of the electronic industry in the recent decades has generated a significant gap between the engineer profile required from the industry and the profile effectively obtained from the university. Nowadays the lack of more practical insight of recent graduates is a serious problem for companies around the world [2].

Hence, the investment of resources on the semiconductors sector (from Brazilian government) has characterized a proper strategy to meet the local market requirements and disseminate technical knowledge and specialized skills in the South America. Under this context, the set of government actions culminated in the creation of the National Training Program for Integrated Circuits IC Designers. Approved in June 2005 by the Committee of Information Technology Area (CATI), the Department of Information Technology Policy (Sepin), and the Ministry of Science, Technology and Innovation (MCTI), the so-called IC-Brazil Program is the result of joint action involving the federal government, private institutions and the academic sector. In this context, the program has the mission of contributing to the creation and organization of a microelectronics ecosystem toward the innovation in products and the inclusion of the country in the semiconductors market.

Considering this proposal for microelectronics education, this paper describes the structure of the training, focusing on the computer environment-based integrated circuits IC design flow. Thus, section II describes the general structure of the training, section III presents the general features of the proposed project (emphasizing the analog module) and section IV summarizes the results and evolution perspectives.

II. Training: General Structure

Resulting from the connection between government agents for organizing and streamlining actions of common interest for the development of the semiconductors sector, the integration and management model around de training program is represented on Fig. 1.

By applying a standard format established along 11 months and planned to have 2 phases (theory and design tools-based training), the program was physically structured from 2 units (training centers) in different country regions.

- Training Center 1 - TC1 (located at Porto Alegre-RS city, within the premises of the Federal University of Rio Grande do Sul - UFRGS);

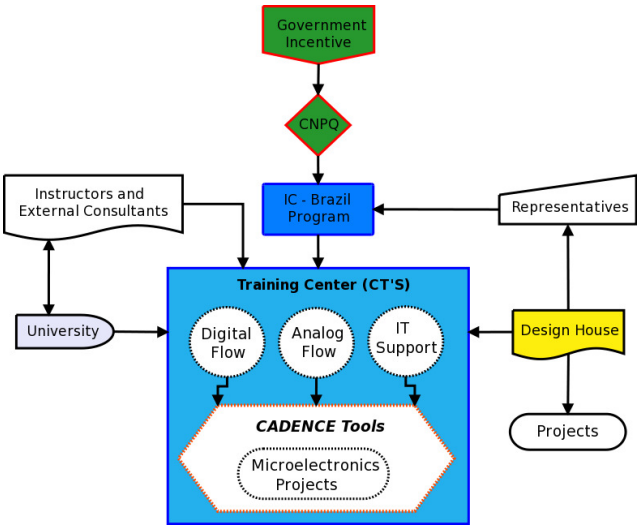

Fig. 1. Training centers: integration and management model.

- Training Center 2 - TC2 (located at Campinas-SP city, within the premises of the Center of Information Technology Renato Archer - CTI).

Comprising a set of concepts involving structure, design theory and computer environment-based design flow, the training is organized according to 3 different options for professional certification:

- Digital systems: digital design flow applied on medium and large structures (dedicated systems and microcontrollers);
- Analog and mixed-signal AMS systems: analog design flow approaching interfacing structures (analog-to-digital converters ADC and digital-to-analog converters DAC);
- Radio frequency RF systems: analog design flow approaching structures for communication at architecture and building block level (transceiver modules: receiver, transmitter and frequency synthesizer).

A. *Phase I*

Representing the theoretical and conceptual phase of the training and developed during 5 months, Phase I is organized through the dynamic connection between 3 parallel processes:

- Lectures to develop theoretical knowledge (electronic components, structures and systems);
- Laboratory activities to develop design environment-based knowledge (analog/digital electronic design flow);
- Project activities to develop effective design skills (EDA tools-based design of electronic structures).

In this context concerning the design, characterization and evaluation of electronic structures (at elementary component and building block level), the proposed sequence of practical activities demonstrates a substantial enhancement in the educational experience [3].

B. *Phase II*

The professional profile required from the semiconductors market has leveraged the implementation of design-based proposals for training [4] [5]. In this context, considering the reference demands and conditions of the semiconductors industry, Phase II promotes a development experience (organized in 6 months) for the students under training from a simulated design environment involving: (1) a management structure, (2) a reference schedule for development and (3) a technical document for project specification.

The adopted management structure (1) can be represented from Fig. 2. Specific for the RF team, the block diagram indicates the set of supervising and design attributions for project development, where each RF instructor is responsible for a specific design team and specific module. A reference schedule (2) for project development is provided through a set of 5 design stages or milestones establishing specific design goals at different abstraction views along the entire analog development flow, according to the Fig. 3. Considering this organizational context for design, the so-called SOW (Statement of Work) is structured as a reference document (3) for project-based activities, providing a set of organizational and technical information, in conformity with the indicated topics:

- Instructors team description (technical support and design coordination);
- Project characterization (general technical description and project specifications, communication protocol and architectures representation at system level);
- Design phases and timeline for activities (dates for expected results - design status and documents);
- Building blocks definition for development.

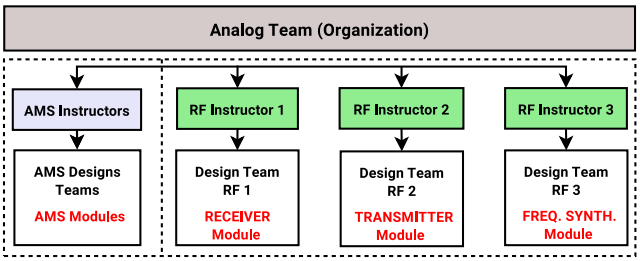

Fig. 2. Phase II: analog team (organization and attributions).

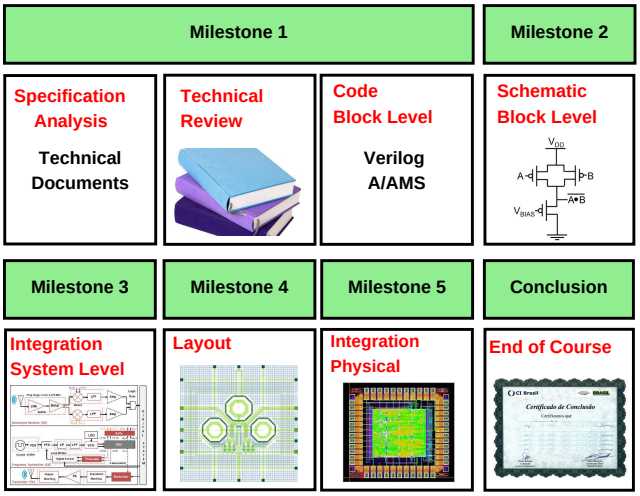

Fig. 3. Phase II: applied sequence of design phases.

III. Project Proposal

Structured as a new project proposal at the context of training Phase II (CT2 - edition 2013), the so-called CACIQ Xavante defines a fully integrated solution (tag and reader) for RFID protocol-based applications. By applying a CMOS-based technology (X-FAB XC 0.18μm), the project involves 3 operating modules for final integration. Digital module is composed by a general purpose microcontroller for the management of the analog (AMS and RF) system operation. AMS module involves a set of building blocks for interfacing and data acquisition operations (voltage reference, comparators and data converters). Finally, representing the focus of this work, RF module involves a complete transceiver specified according to ISO/IEC 18000-4 (2.45 GHz air interface) at ISM (Industrial, Scientific and Medical) band. Thus, the set of resulting technical features can be summarized according to the following topics:

- Modulation Scheme: OOK (On-Off Keying)
- Frequency Range: 2.4 GHz to 2.475 GHz
- Channel Spacing: 5 MHz
- Number of Channels: 16
- Baseband frequency: 50 kHz

According to the Fig. 4 (complete RF transceiver block diagram), the reference architecture for implementation is composed through 3 sub-modules [6]: (1) a homodyne receiver for signal acquisition, (2) a direct conversion transmitter for signal transmission, and (3) a type II third-order phase locked loop PLL-based frequency synthesizer for reference frequency generation (local oscillator) for signal frequency translation at receiver and transmitter chain.

Considering this proposal, under a technical point of view, the resulting environment for project development at training context is driven to enable 2 design approaches (according to development context): (1) redesign and optimization of structures according to predefined solutions, and (2) research and proposition of alternative solutions for pending questions or features to be improved.

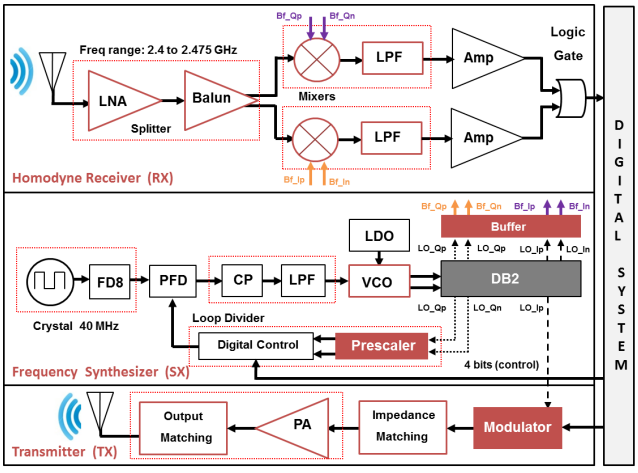

Fig. 4. RFID protocol-based transceiver: complete block diagram.

Considering the second approach, Fig. 5 represents the application conditions around the divide-by-2 circuit DB2, building block (from frequency synthesizer) implemented through current mode logic CML-based topology for output frequency generation [7] [8] [9] [10] [11]. In this case, the corresponding connection diagram (Fig. 5) illustrates a specific critical point for design to be solved: driving of multiple loads with unbalanced structure and input impedance (receiver, transmitter and PLL feedback path) and operation with optimized power consumption.

IV. Results

The set of obtained results can be summarized considering three basic production factors: (1) technical documentation, (2) project conclusion (layout level physical implementation) and (3) learning elements (personal experience, knowledge and design skills).

The first production factor (technical documentation) can be described through the material generated along the milestones for each trainee, in conformity with the design phase (by applying predefined reference templates), as follows:

- Block Guide: description about front end design (behavioural/structural modeling, simulation results);
- Test Guide: description of the structures and strategies for test and testability;
- Layout Guide: information about backend design (pin dimensions and layout strategies);
- IP Brief: summary of technical information about structure (topology and pin description) and operation (performance parameters and electrical characteristics).

The second production factor represents the set of concrete results obtained from direct design effort. In this context, the EDA tools-based reference electronic design flow (presented during Phase I) was applied along the Phase II milestones for generating a final physical implementation (layout level design). As a result, Fig. 6 illustrates a RF building block-based example: layout implementation for divide-by-2 circuit DB2 with unbalanced sizing, which is the proposed solution for the pending technical question indicated from Fig. 5 [12] [13] [14].

Finally, the third production factor derived from the training is given through the learning elements resulting from design experience. Thus, the maturation condition developed during design flow stimulates the perception about different approaches concerning process views (conditions and limitations).

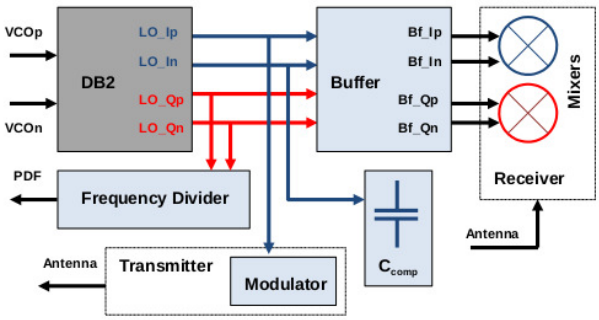

Fig. 5. Divide-by-2 circuit: complete connection diagram.

Stimulated through trainee experience phase, according to Fig 7, the perception of hierarchy views refers to different structure levels, and the perception of abstract views refers

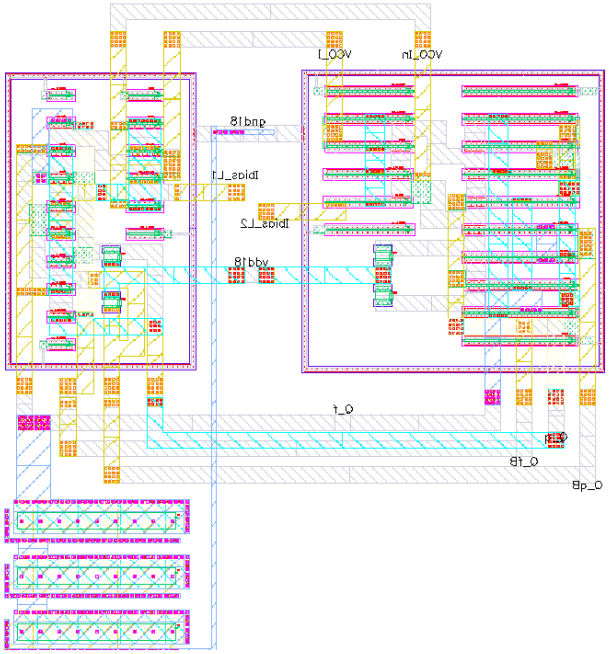

Fig. 6. Divide-by-2: final layout level implementation.

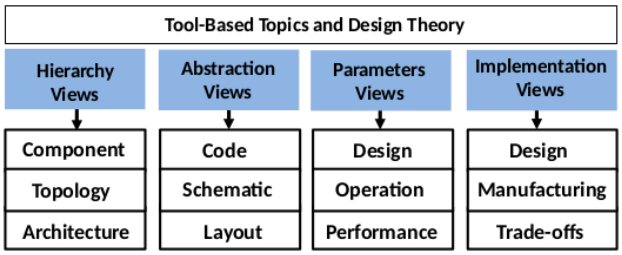

Fig. 7. Different approaches for the perception of IC design process.

to different design phases. Additionally, parameters views establish a cause-effect relationship between structural features, operating conditions and corresponding performances, and finally, implementation views refers the different phases and processes for integrated circuit conception.

V. Conclusion

Considering the microelectronics development scenery, IC-Brazil Program has represented an initiative of professional certification for providing a local availability of suitable design skills to meet the demands of the semiconductors development industry. Characterized and particularized in this work through the presented design examples, the edition 2013 represented the forth training experience at CT2 with the referred structure.

Assuming a student perspective, the training provides technical and human experiences. Under a technical point of view, the set of experiences involves convergence between practice and theory through an EDA tools-based project specification along the entire electronic design flow, implemented through a simulated development environment (reflecting industry features). The set of actions addressed from design attributions involves technical documentation analysis, additional research and performance comparison for different electronic structures, final modules integration and parallel generation and updating of corresponding documentation with a complete description about design history.

Under a human point of view, the set of experiences involves a dynamic interaction between project coordinators, designers and work teams toward the final project integration (at building block level, architecture level and system level). Along the development process chain, the adopted model for design verification and management is based on the procedures applied in a real work environment.

The development of this process has created along the time a promising perspective for the approximation between the background of the professional certified through the training and the effective needs of the IC design market.

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